



12-Bit, 65 MSPS Monolithic A/D Converter

AD6640

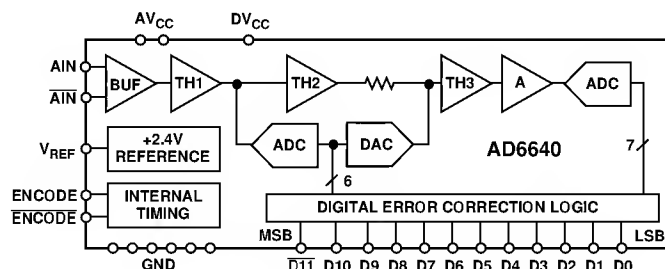
FEATURES

- 65 MSPS Minimum Sample Rate
- 80 dB Spurious-Free Dynamic Range
- IF-Sampling to 70 MHz
- 695 mW Power Dissipation
- Single +5 V Supply
- On-Chip T/H and Reference
- Twos Complement Output Format
- 3.3 V or 5 V CMOS-Compatible Output Levels

APPLICATIONS

- Cellular/PCS Base Stations
- Multichannel, Multimode Receivers
- GPS Anti-Jamming Receivers
- Communications Receivers

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD6640 is a high speed, high performance, low power, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference are included on-chip to provide a complete conversion solution. The AD6640 runs on a single +5 V supply and provides CMOS-compatible digital outputs at 65 MSPS.

Specifically designed to address the needs of multichannel, multimode receivers, the AD6640 maintains 80 dB spurious-free dynamic range (SFDR) over a bandwidth of 25 MHz. Noise performance is also exceptional; typical signal-to-noise ratio is 68 dB.

The AD6640 is built on Analog Devices' high speed complementary bipolar process (XFCB) and uses an innovative multipass architecture. Units are packaged in a 44-terminal Thin Quad Plastic Flatback (TQFP) specified from -40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate is 65 MSPS.
2. Fully differential analog input stage specified for frequencies up to 70 MHz; enables "IF-Sampling."
3. Low power dissipation: 695 mW off a single +5 V supply.
4. Digital outputs may be run on +3.3 V supply for easy interface to digital ASICs.
5. Complete Solution: reference and track-and-hold.
6. Packaged in small, surface mount, plastic 44-terminal TQFP.

REV. 0

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AD6640- SPECIFICATIONS

DC SPECIFICATIONS (AVCC = +5 V, DVCC = +3.3 V; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	Min	AD6640AST Typ	Max	Units
RESOLUTION				12		Bits
ACCURACY				GUARANTEED		
No Missing Codes	Full	VI				
Offset Error	Full	VI	-10	±3.5	+10	mV
Gain Error	Full	VI	-10	4.0	+10	% FS
Differential Nonlinearity (DNL)	Full	VI	-1.0	±0.3	+1.5	LSB
Integral Nonlinearity (INL)	Full	V		±1.5		LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		10		ppm/°C
Gain Error	Full	V		100		ppm/°C
POWER SUPPLY REJECTION (PSRR)	Full	V		±0.5		mV/V
REFERENCE OUT (VREF) ¹	+25°C	V		2.4		V
ANALOG INPUTS (AIN, $\overline{\text{AIN}}$)						
Differential Input Voltage Range	Full			2.0		V p-p
Differential Input Resistance	Full	IV	0.7	0.9	1.1	kΩ
Differential Input Capacitance	+25°C	V		1.5		pF
POWER SUPPLY						
Supply Voltage						
AVCC	Full	VI	4.75	5.0	5.25	V
DVCC	Full	VI	3.0	3.3	5.25	V
Supply Current						
I _{AVCC} (AVCC = 5.0 V)	Full	V				mA
I _{DVCC} (DVCC = 3.3 V)	Full	V				mA
Total I _{CC}	Full	VI		139	175	mW
POWER CONSUMPTION	Full	VI		695	875	mW

NOTES

¹TO COME.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AVCC = +5 V, DVCC = +3.3 V; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	Min	AD6640AST Typ	Max	Units
LOGIC INPUTS (ENC, $\overline{\text{ENC}}$) ¹						
Differential Input Voltage	Full	IV	0.4	1.0	5.0	V
Logic Compatibility ²	Full	IV		TTL/CMOS		
Logic "1" Voltage	Full	VI	2.0		5.0	V
Logic "0" Voltage	Full	VI	0		0.8	V
Logic "1" Current (V _{INH} = 5 V)	Full	VI	450	625	800	μA
Logic "0" Current (V _{INL} = 0 V)	Full	VI	-400	-300	-200	μA
Input Capacitance	+25°C	V		2.5		pF
LOGIC OUTPUTS ($\overline{\text{DII}}$ -D0)						
Logic Compatibility				CMOS		
Logic "1" Voltage (DVCC = +3.3 V)	Full	VI	2.5	2.9		V
Logic "0" Voltage (DVCC = +3.3 V)	Full	VI		0.25	0.8	V
Logic "1" Voltage (DVCC = +5.0 V)	Full	IV	4.0	4.6		V
Logic "0" Voltage (DVCC = +5.0 V)	Full	IV		0.4	0.8	V
Output Coding				Two's Complement		

NOTES

¹TO COME.

²TO COME.

SWITCHING SPECIFICATIONS (AVCC = +5 V, DVCC = +3.3 V; ENCODE & $\overline{\text{ENCODE}}$ = 65 MSPS; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	Min	AD6640AST Typ	Max	Units
Maximum Conversion Rate	Full	VI	65			MSPS
Minimum Conversion Rate	Full	IV			5	MSPS
Aperture Delay (t _A)	+25°C	V		-250		ps
Aperture Uncertainty (Jitter)	+25°C	V		0.3		ps rms
ENCODE Pulse Width High ¹	+25°C	IV	7			ns
ENCODE Pulse Width Low	+25°C	IV	7			ns
Output Delay (t _{OD}) DVCC +3.3 V ²	Full	IV	4.2	6.0	8.6	ns
Output Delay (t _{OD}) DVCC +5.0 V	Full	IV	4.0	8.0	14.0	ns

NOTES

¹All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.

²Analog Input signal power swept from -20 dBFS to -95 dBFS; Dither power = -32.5 dBm.

Specifications subject to change without notice.

AC SPECIFICATIONS¹ (AVCC = +5 V, DVCC = +3.3 V; ENCODE & $\overline{\text{ENCODE}}$ = 65 MSPS; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	Min	AD6640AST Typ	Max	Units
SNR						
Analog Input 2.2 MHz	+25°C	V		68		dB
@ -1 dBFS 15.5 MHz	+25°C	I	64	67		dB
31.0 MHz	+25°C	V		67		dB
69.0 MHz	+25°C	V		66		dB
SINAD						
Analog Input 2.2 MHz	+25°C	V		67.5		dB
@ -1 dBFS 15.5 MHz	+25°C	I	63.5	66.5		dB
31.0 MHz	+25°C	V		66.5		dB
69.0 MHz	+25°C	V		65		dB
Worst Harmonic (2nd or 3rd)						
Analog Input 2.2 MHz	+25°C	V		80		dBc
@ -1 dBFS 15.5 MHz	+25°C	I	74	80		dBc
31.0 MHz	+25°C	V		79		dBc
69.0 MHz	+25°C	V		77		dBc
Worst Harmonic (4th or Higher)						
Analog Input 2.2 MHz	+25°C	V		86		dBc
@ -1 dBFS 15.5 MHz	+25°C	V		86		dBc
31.0 MHz	+25°C	V		85		dBc
69.0 MHz	+25°C	V		84		dBc
Multitone SFDR (w/Dither) ²						
Eight Tones @ -20 dBFS	Full	V		90		dBFS
Two-Tone IMD Rejection						
F1, F2 @ -7 dBFS	Full	V		80		dBc
Analog Input Bandwidth	+25°C	V		240		MHz
Transient Response	+25°C	V		10		ns
Overvoltage Recovery Time	+25°C	V		20		ns

NOTES

¹All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.

²Analog Input signal power swept from -20 dBFS to -95 dBFS; Dither power = -32.5 dBm.

Specifications subject to change without notice.

AD6640

WAFER TEST LIMITS¹ ($AV_{CC} = DV_{CC} = +5\text{ V}$; ENCODE = 20 MSPS unless otherwise noted)

Parameter	Temp	AD6640CHIPS		Units
		Min	Max	
POWER SUPPLY I_{CC} Supply Current	+25°C	100	175	mA
ENCODE Input Logic "1" Current	+25°C	450	800	μA
Logic "0" Current	+25°C	-400	-200	μA
DC ACCURACY Offset Error	+25°C	-10	10	mV
Gain Error	+25°C	-10	10	% FS
No Missing Codes	+25°C	Guaranteed		
Differential Nonlinearity	+25°C	-0.995		LSB

NOTES

¹Electrical test is performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice.

²Die substrate is connected to 0 V.

ABSOLUTE MAXIMUM RATINGS¹

Parameter	Min	Max	Units
ELECTRICAL			
AV_{CC} Voltage	0	7	V
DV_{CC} Voltage	0	7	V
Analog Input Voltage	0.5	4.5	V
Analog Input Current		20	mA
Digital Input Voltage (ENCODE)	0	AV_{CC}	V
ENCODE, ENCODE Differential Voltage		4	V
Digital Output Current	-40	40	mA
ENVIRONMENTAL ²			
Operating Temperature Range (Ambient)	-40	+85	°C
Maximum Junction Temperature		+150	°C
Lead Temperature (Soldering, 10 sec)		+300	°C
Storage Temperature Range (Ambient)	-65	+150	°C

NOTES

¹Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

²Typical thermal impedances (44-terminal TQFP); $\theta_{JA} = 55^\circ\text{C}/\text{W}$.

EXPLANATION OF TEST LEVELS

Test Level

- I - 100% production tested.
- II - 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
- III - Sample tested only.
- IV - Parameter is guaranteed by design and characterization testing.
- V - Parameter is a typical value only.
- VI - All devices are 100% production tested at +25°C; sample tested at temperature extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6640AST	-40°C to +85°C (Ambient)	44-Terminal TQFP (Thin Quad Plastic Flatpack)	ST-44
AD6640CHIPS	-40°C to +85°C (Ambient)	Unpackaged Die	
AD6640ST/PCB		Evaluation Board with AD6640AST	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6640 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1, 2	DV _{CC}	+3.3 V/+5 V Power Supply (Digital). Powers output stage only.
3	ENCODE	Encode input. Data conversion initiated on rising edge.
4	$\overline{\text{ENCODE}}$	Complement of ENCODE. Drive differentially with ENCODE or bypass to Ground for single-ended clock mode.
5, 6	GND	Ground.
7	AIN	Analog Input.
8	$\overline{\text{AIN}}$	Complement Analog Input.
9	V _{REF}	Internal Voltage Reference. Nominally +2.4 V. Bypass to Ground with 0.1 μF + 0.01 μF microwave chip cap.
10	C1	Internal Bias Point. Bypass to ground with 0.01 μF cap.
11, 12	AV _{CC}	+5 V Power Supply (Analog).
13, 14	GND	Ground.
15, 16	AV _{CC}	+5 V Power Supply (Analog).
17, 18	GND	Ground.
19, 20	AV _{CC}	+5 V Power Supply (Analog).
21, 22	GND	Ground.
23	NC	No Connect.
24	GND	Ground.
25	D0 (LSB)	Digital Output Bit (Least Significant Bit)
26–33	D1–D8	Digital Output Bits
34, 35	GND	Ground.
36, 37	DV _{CC}	+3.3 V/+5 V Power Supply (Digital). Powers output stage only.
38, 39	GND	Ground.
40, 41	DV _{CC}	+3.3 V/+5 V Power Supply (Digital). Powers Output Stage only.
42, 43	D9–D10	Digital Output Bits.
44	$\overline{\text{D11}}$ (MSB) ¹	Digital Output Bit (Most Significant Bit).

NOTE

¹Output coded as twos complement.

PIN CONFIGURATION

